CLAIMS

What is claimed is:

1. A memory interface comprising:

an inductor; and

a plurality of transmission lines, coupled to the inductor in series, to couple a plurality of memory devices to a circuit board.

2. The memory interface of claim 1, further comprising:

one or more impedance transformers coupled to the inductor in series.

3. The memory interface of claim 2, wherein one or more of the plurality of transmission lines are used as the one or more impedance transformers.

4. The memory interface of claim 1, wherein the plurality of memory devices comprises one or more synchronous dynamic random access memories (SDRAMs) operable at a frequency above 200 MHz.

5. A method to interface a circuit board with a plurality of memory devices, the method comprising:

coupling the plurality of memory devices to a semiconductor device by circuitry, the circuitry including an inductor.

6. The method of claim 5, wherein the circuitry is fabricated on the circuit board and the semiconductor device is a memory controller mounted on the circuit board.

7. The method of claim 6, wherein the circuitry further comprises a resistor coupled to the inductor in series.

8. The method of claim 5, wherein the circuitry comprises a plurality of transmission lines coupled to the inductor in series on the circuit board.

9. The method of claim 8, wherein the plurality of transmission lines comprises one or more impedance transformers.

10. The method of claim 5, wherein the plurality of memory devices includes one or more synchronous dynamic random access memories (SDRAMs) operable at a frequency above 200 MHz.

11. A method to design a memory interface comprising:

performing topology optimization in frequency domain to determine a value of an inductor to be coupled in series with a plurality of transmission lines in the memory interface; and

performing sensitivity analysis to fine-tune the value of the inductor.

12. The method of claim 11, wherein sensitivity analysis comprises statistical simulation in time domain.

13. The method of claim 11, further comprising generating a model in response to result of the topology optimization and the sensitivity analysis.

14. The method of claim 13, further comprising simulating the model in time domain to generate a design of the memory interface.

15. A computer system comprising:

a plurality of synchronous dynamic random access memories (SDRAMs);

a memory controller; and

a memory interface coupling the memory controller to the plurality of SDRAMs, the memory interface comprising

an inductor, and

a plurality of transmission lines coupled to the inductor.

16. The computer system of claim 15, wherein the memory interface further comprises a resistor coupled to the inductor in series.

17. The computer system of claim 15, wherein the plurality of transmission lines includes one or more impedance transformers.

18. The computer system of claim 15, further comprising a processor coupled to the memory controller.

19. The computer system of claim 15, wherein the plurality of SDRAMs includes a double-data rate (DDR) SDRAM device.

20. A memory interface comprising:

an impedance transformer to couple a synchronous dynamic random access memory (SDRAM) to a motherboard in a computer system.

21. The memory interface of claim 20, wherein the impedance transformer is a multi-section impedance transformer.

22. The memory interface of claim 20, wherein the speed of the SDRAM is over 200 MHz.

23. The memory interface of claim 20, further comprising a plurality of transmission lines, wherein one the plurality of transmission lines is used as the impedance transformer.

24. A machine-accessible medium that provides instructions that, if executed by a processor, will cause the processor to perform operations comprising:

performing topology optimization in frequency domain to determine a value of an inductor to be coupled in series with a plurality of transmission lines in the memory interface; and

performing sensitivity analysis to fine-tune the value of the inductor.

25. The machine-accessible medium of claim 24, wherein the operations further comprise:

generating a model in response to result of the topology optimization and the sensitivity analysis.

26. The machine-accessible medium of claim 25, wherein the operations further comprise simulating the model in time domain to generate a design of the memory interface.